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EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/540,022	MIZUGUCHI ET AL.	
	Examiner	Art Unit	
	SIU M. LEE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9 and 11-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 5-9, 11-17,* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 15 recites “wherein the integer is a multiple of four; and the predetermined number of clock is a number of clocks in which the number is obtained by multiplying one-fourth with the multiple of four”. Claim 15 depend on claim 5 and claim 5 depends on claim 1.

The “integer” recites in claim 15 is the "integral multiple” as recite in claim 1, which is the oversampling frequency generate by the multiplication PLL 120 in figure 2. From the specification, the multiplier used is 16 times to generate a 400 MHz clock from a 25 MHz clock as shown in figure 2.

The “predetermined number of clock” is the clock delayed by the timing adjustment section 210 as discloses in page 20, lines 20-23, “the timing adjustment section 210 delays the clock, which indicates the zero cross points detected by the zero cross detection section 205, by eight clock, and output the 25 MHz clock C indicating

timings for symbol points". When we multiply one-fourth with the multiple of four (16 in this case), the result is 4 instead of 8 as discloses in figure 8. It is contradicting with the teaching in figure 8 and 13.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2 ,5-9, 11-14, 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen et al. (Nguyen) (US 6,493,396 B1) in view of .

(1) Regarding claims 1 and 16:

Nguyen discloses a system having a symbol of a data signal transmitted based on a first clock signal having a predetermined frequency, the device comprising:

high frequency clock signal generation means (XCO 230, ramp generator 220, and comparator 210 in figure 5) for generating a second clock signal having a frequency of an integral multiple of a frequency of the first clock signal (analog-to-digital converter 425 samples each of the I and Q signals using a sampling clock of 20.736 megaHertz, preferably the synchronized clock signal 235 of FIG. 5, column 7, lines 3-6);

data value acquisition means for acquiring a data value of the data signal based on timing of the second clock signal generated by the high frequency clock signal

generation means (analog-to-digital converter 425 samples each of the I and Q signals at a sampling rate that is preferably 16 times the symbol rate, column 7, lines 1-2);

zero cross detection means (transition detector 445 in figure 7) for detecting, as a zero cross point, a timing at which a magnitude relationship with respect to a predetermined criterion level inverted for the component of the first clock signal extracted by the clock component extraction means (transition detector 445 to determine the time of occurrence of a transition in the particular signal being monitored, either I or Q. When the transition detector 445 detects a transition of the monitored signal, a sync pulse is generated at line 450. Preferably, a state machine is used to detect a zero crossing transition by searching for a transition pattern in five consecutive samples, column 7, lines 25-32, it is inherent for a zero crossing detection to detect a timing when a magnitude relationship with respect to a predetermined criterion level inverted between the previous sample and the present sample); and

symbol position detection means (clock generator 470 in figure 7) for detecting, as a symbol position of the data signal, a time when a time period corresponding to a predetermined number of clocks for the second clock signal is elapsed from the zero cross point detected by the zero cross detection means (the symbol clock pulse that is generated by the clock generator 470 is located at the center of the symbol, column 8, lines 3-5; as the symbol is oversampled by 16 times, therefore, the symbol location is in the center (8 samples) after the zero crossing);

wherein the zero cross detection means detects as the zero cross point, a clock whose position corresponding to a timing closest to the timing at which the magnitude

relationship with respect to the predetermined criterion level is inverted for the first clock component extracted by the clock component extraction means (it is inherent for a zero crossing detection to detect a timing when a magnitude relationship with respect to a predetermined criterion level inverted between the previous sample and the present sample).

Nguyen fails to disclose a clock component extraction means for extracting a component of the first clock signal from the data value acquired by the data value acquisition means.

However, Imanaka discloses a clock component extraction means (waveform equalizer 13 in figure 1) for extracting a component of the first clock signal from the data value acquired by the data value acquisition means (waveform equalizer 13 reshape the digital data converted in the A/D converter, the wave equalizer has a digital filter for heightening a gain of an attenuated high-frequency signal component of the digital signal, paragraph 0037, lines 9-14).

It is desirable to have a clock component extraction means for extracting a component of the first clock signal from the data value acquired by the data value acquisition means because it reshape the attenuated high-frequency signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Imanaka in the system of Nguyen to improve the quality of the sampled signal.

(2) Regarding claims 2 and 17:

Nguyen discloses wherein the data signal is a signal in which the magnitude relationship with respect to the predetermined criterion level is alternately inverted from symbol to symbol (as discloses in figure 2, the I (20) and Q (25) signal having the magnitude relationship with respect to the predetermined criterion level is alternately inverted from symbol to symbol).

(3) Regarding claim 5:

Nguyen discloses wherein the clock determined as being at a position of the symbol in the data signal by the symbol position detection means is at a timing at which the predetermined number of clocks is passed from the zero cross point (the symbol clock pulse that is generated by the clock generator 470 is located at the center of the symbol, column 8, lines 3-5; as the symbol is oversampled by 16 times, therefore, the symbol location is in the center (8 samples) after the zero crossing).

(4) Regarding claim 6:

Nguyen discloses wherein the symbol position detection means outputs a third clock signal with a timing when the symbol position is detected (the clock generator circuit 470 generates a symbol clock RSYMBOL (1296 MHz) as shown in figure 7, column 7, lines 54-57).

(5) Regarding claim 7:

Nguyen discloses wherein the zero cross detection means outputs the third clock signal when the time period corresponding to the predetermined number of clocks is elapsed from the zero cross point (the I and Q data is sample by the analog-to-digital converter 425 with a sampling rate of 16 times of the I and Q data rate; that is 20736

MHz, therefore the data rate of I and Q data is 1296 MHz, column 7, lines 1-5; as the transistor detector detects the zero crossing and send out a sync pulse represent a zero crossing has been detected, it is equivalent to a clock signal of 1296 MHz when 16 clocks elapsed from the zero cross point).

(6) Regarding claim 8:

Nguyen discloses a determination means (voter circuit 420 and QPSK decoding 490 in figure 7) for determining a data value of the symbol in the data signal, based on timing of the third clock signal outputted by the symbol position detection means (clock generator 470 supply the RSYMBOL_CLK to the voter circuit 420 and QPSK decoder 490) (voter circuit 420 is used to determine the polarity of the sign bit for each of the I and Q components of the received signal based on RSYMBOL_CLK and output the result to QPSK decoding 490, QPSK decoder circuit 490 analyzes the last and present I and Q outputs from the voter circuit 420 and reconstructs the initial data bit pair. This pair is passed on to a parallel to serial converter in the decoder 490 where the received data stream is reconstructed, column 8,, lines 20-25, 51-53).

(7) Regarding claim 9:

Nguyen discloses the system comprising:

output clock signal generation means (the clock generator 470 generates a data clock RCLK as shown in figure 7, column7, lies 54-56) for generating a low jitter fourth clock signal (RCLK of 2592 MHz); and

output means (preamble pattern detector 50 in figure 7) for externally outputting the data value determined by the determination means, based on the fourth clock signal

generated by the output clock signal generation means (clock generator 470 supply the RCLK to the preamble pattern detector 500) (preamble pattern detector 500 output the RDATA at output line 415 of the preamble pattern detector 500, column 9, lines 28-29).

(8) Regarding claim 11:

Nguyen discloses wherein the zero cross detection means detects, as the zero cross point, the timing at which the "positive"/"negative" sign of the first clock signal component is inverted (the sign bits of either the I or Q sampled signals, RI(5) or RQ(5), are supplied to the input of a transition detector 445 to determine the time of occurrence of a transition in the particular signal being monitored, column 7, lines 24-27).

(9) Regarding claim 12:

Nguyen discloses wherein the data signal is a signal in which the "positive"/"negative" sign of the data value is alternately inverted from symbol to symbol (as discloses in figure 2, the I (20) and Q (25) signal having the magnitude relationship with respect to the predetermined criterion level is alternately inverted from symbol to symbol).

(10) Regarding claim 13:

Nguyen discloses wherein output clock generation means generates the fourth clock signal on the basis of the third clock signal (the clock generator circuit 470 preferably includes a counter or a state machine that is progressively advanced by the phased clock signal CLK_20 (e.g., 20.736 MHz) to generate the data clock RCLK (e.g., 2.592 MHz) and symbol clock RSYMBOL_CLK (e.g., 1.296 MHz) signals based on the timing of the sync pulses received from the peak detector 460, column 7, lines 52-58).

(11) Regarding claim 14:

Nguyen discloses wherein the integer is a multiple of four (16 times, column 7, lines 1-2).

Allowable Subject Matter

3. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. (US 2003/0041292 A1) discloses a data recovery circuit for minimizing power consumption by non0integer times oversampling. Yang et al. (US 6,940,926 B1) discloses a digital phase/frequency detector. Valleet et al. (US 7,180,966 B2) discloses transition detection, validation and memorization circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIU M. LEE whose telephone number is (571)270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Siu M Lee/
Examiner, Art Unit 2611
4/9/2008

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611